

Output Voltage and Current Waveforms' PSIM Simulation of Three-Phase Seven-Level Cascaded H-Bridge Inverter

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Abstract—The paper considers a PSIM model of the seven-level cascaded H-bridge voltage source inverter, including a control circuits of its power switches (on the base signals' level). This simplified PSIM model is intended only for the investigation of the inverter output voltages and currents quality (the harmonic content, namely voltages' and currents' THD and voltages' weighted THD), since the used here first level of the model supposes a simple and strict correspondence between coordinates of specified space vectors' and the power switches' states. A way of using this kind of PSIM models with minimum changes for simulation of multilevel voltage source inverters (MLVSI) under both the carrier-based PWM and some kinds of space vector PWM is demonstrated. By way of illustration the dependences of some of the above mentioned harmonic coefficients on the amplitude modulation index are shown and the approach to supplementing the inverter model control circuit for the common-mode voltage minimization and the related waveforms are presented.

Keywords—multilevel voltage source inverters, seven-level three-phase inverter, cascaded H-bridge inverter, carrier-based PWM, quarter-wave-symmetric space vector PWM, THD, integrated voltage harmonics factors, weighted THD, common-mode voltage, PSIM simulation

I. INTRODUCTION

In recent years, industrial application of multilevel voltage source inverters (MLVSI) has reached a new level, thanks to progress in both the power switches technology and affordability of the control unit components, namely DSP and FPGA. MLVSI are gaining their niche in many applications, reaching the medium and high values of rated output voltage and power [1-7]. Inverters with a relatively low number of levels are particularly attractive for simulations, mock-up researches and industrial implementations, since they are not yet critically complicated to control and do not require expensive solutions, but offer important opportunities for experiments with carrier-based, space vector and mixed kinds of PWM. Many papers have been published regarding both classical and modified circuitry and control solutions for seven-level voltage source inverters, see for instance [8-11].

The three-phase cascaded H-bridge inverters (CHBI) are probably the most used kind of MLVSI due to they can be aggregated from the thoroughly studied cells, which run by a simple principle. A PSIM-model of phase "A" power circuit of the three-phase seven-level CHBI is shown in Fig. 1. The power switches' gate states (signals), which are suitable and conventional for H-bridge switching states generating, are shown in Table I. To reduce the number of the IGBTs commutations, the two switching states of the zero vector for positive and negative voltage half-waves can be used.

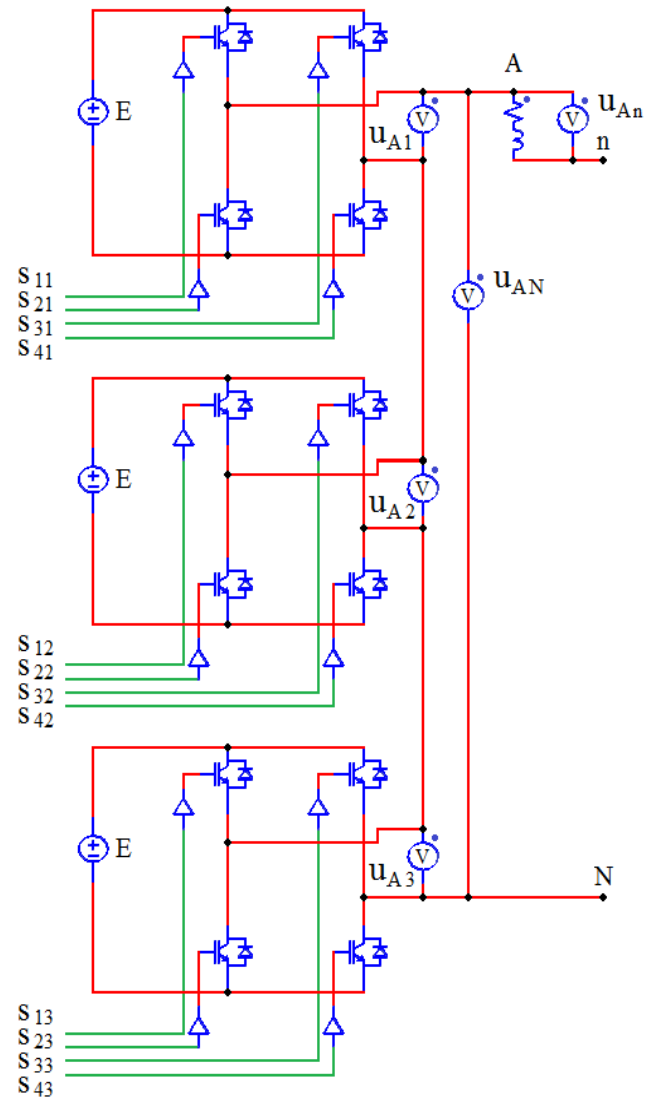


Fig. 1. PSIM-model of phase A power circuit of three-phase seven-level cascaded H-bridge inverter.

TABLE I. H-BRIDGE OUTPUT VOLTAGE GENERATING

Power Switches' Gate States of H-Bridge with Number i ($i = 1, 2, 3$)				H-Bridge Output Voltage u_{Ai}^*
S_{1i}	S_{2i}	S_{3i}	S_{4i}	
1	0	1	0	0
0	1	0	1	0
1	0	0	1	1
0	1	1	0	-1

Here and after all the inverter phase voltages u_X and delta voltages u_{XY} (including the values with any additional subscript designations) are treated as having also the relative (normalized) values, which are marked with asterisks:

$$u_X^* = \frac{u_X}{U_d} = \frac{u_X}{E}, \quad u_{XY}^* = \frac{u_{XY}}{U_d} = \frac{u_{XY}}{E}, \quad (1)$$

where $U_d = E$ is the direct voltage of the unit (base) level.

The resulting phase leg A inverter output voltage with reference to the inverter neutral point N is the combination of H-bridges output voltages u_{Ai}^* :

$$u_{AN}^* = u_{A1}^* + u_{A2}^* + u_{A3}^*. \quad (2)$$

As can be seen from Table I, the bridge zero-voltage state can be obtained by the two tantamount switching combinations. So we have the four useful bridge switching states, and the three of them generate the different bridge output voltages. Also we can talk about the phase switching combinations, whose number is $3^3=27$, and they generate the seven different phase output voltage levels. In turn, the whole seven-level CHBI produces $27^3=19683$ switching combinations, $7^3=343$ switching states and $3 \cdot 7(7-1)+1=127$ vectors. All the vectors are the vertices of the triangles of the vector diagram in Fig. 2, where some of them are shown as (u_{AB}^*, u_{BC}^*) vectors of oblique-angled coordinate system.

II. PURPOSE OF PAPER

The purpose of this paper is to describe basic details of the PSIM model of a power circuit and switches' control interface of the three-phase seven-level cascaded H-bridge inverter (CHBI) and to demonstrate the model simulation capability. The model is intended for the research of a quality of the output voltages without considering processes in power circuit itself. Thus, the choice of switching states between alternatives for the same vector of the phase leg and the use of redundant states remain beyond the responsibility of the model. The PSIM model also makes it possible to investigate the output current waveform and its THD under various CHBI control modes and kinds of generalized loads.

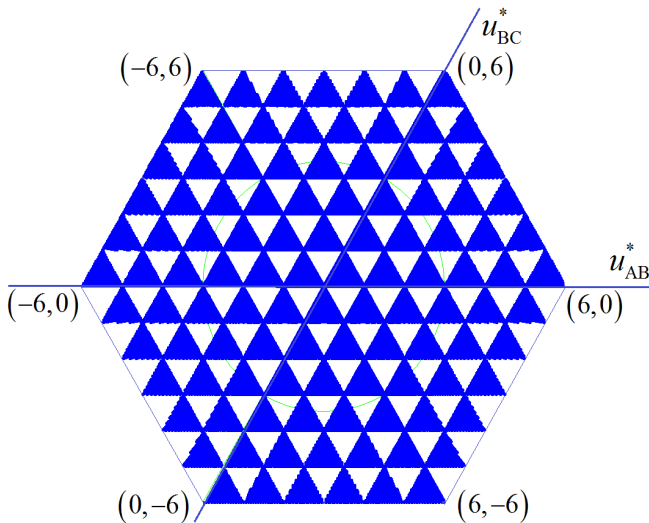


Fig. 2. Full range of vectors of three-phase seven-level inverter.

Also, by way of illustration, the mathematical model for a supplementary unit to inverter model control circuit for the common-mode voltage minimization and the related simulated voltages waveforms are presented.

III. SWITCHES' CONTROL MODEL

The power semiconductor switches PSIM models parameters, like the saturation voltage, the transistor resistance, the anti-parallel diode threshold voltage and resistance can be customized, otherwise, the switches (IGBT, MOSFET, etc.) can be treated as the ideal ones in the power circuit model of Fig. 1. The generalized load's kind and parameters are also being customized, and DC power sources with smoothing filter capacitors can be simulated instead of the shown ideal DC voltage sources.

Given that the used here first level of the model should be a simple and providing some strict correspondence between specified space vectors (space vectors' coordinates) and the power switches' states, we can set the acting of the phase legs' bridges for the phase output voltage generating in accordance with Table II. Correspondingly, the conventional multicarrier sinusoidal PWM (SPWM) for MLVSI is being implemented as shown in Fig. 3.

Here Vmod is the modulating phase voltage signal of the sine waveform, Vmodabs corresponds to the absolute value of the latter; C0=1 for the positive half-waves of Vmod; Vp1...Vp3 are the level-shifted triangle carriers signals and Cp1...Cp3 are the related comparators' signals.

Probably, the most popular and easily implemented kind of the multicarrier SPWM is the phase opposition disposition (POD) [5, 12-15]. In the POD, the carriers of each of the groups (positive and negative) are in phase, but between the groups there is the 180 degrees phase shift. The control waveforms of the POD variant, having 0 degrees phase delay of the positive carrier triangular waves, is shown in Fig. 4.

TABLE II. PHASE LEG OUTPUT VOLTAGE GENERATING

Phase Leg Output Voltage u_{AN}^*	H-Bridges Output Voltages		
	u_{A1}^*	u_{A2}^*	u_{A3}^*
0	0	0	0
± 1	± 1	0	0
± 2	± 1	± 1	0
± 3	± 1	± 1	± 1

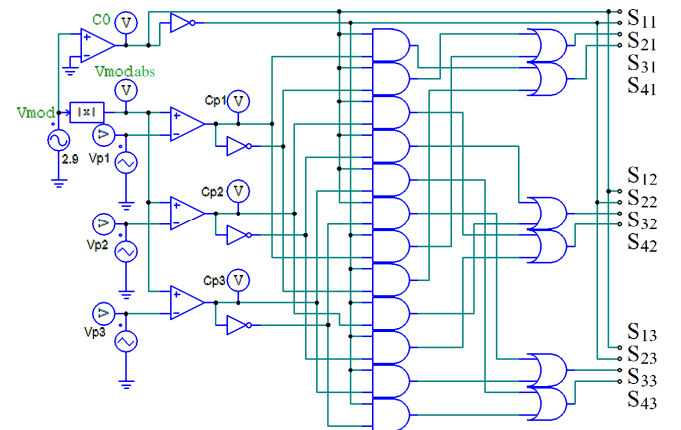


Fig. 3. PSIM-model of phase "X" switches' control interface of three-phase seven-level cascaded H-bridge inverter with multicarrier sinusoidal PWM control.

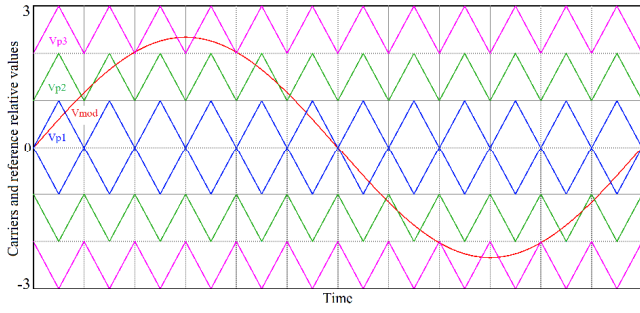


Fig. 4. Phase opposition disposition technique for seven-level inverter.

The using of Vmodabs signal with taking into account the sign of Vmod allowed the number of the triangle carriers signals to be reduced from 6 to 3 in the circuit of Fig. 3, compared the POD implementation shown in Fig. 4.

Obviously, any phase-shifted and level-shifted techniques can be simulated in the same model after appropriate adjust settings for the carriers signals.

The description of some PWM techniques and other modulating techniques is available by means of the so-called executed voltages' signals. These are the resulting control signals after applying the being considered control technique, and their waveforms must be replicated in an appropriate voltage of a power circuit. In other words, they take values that we have chosen from among the accessible values related to the existing set of space vectors and we should provide these values thanks to the control technique.

For example, level-shifted carrier-based modulating techniques, including the above POD multicarrier SPWM modulation technique, can be described by the following expression for the executed output phase voltage u_{XNex}^* of phase "X" with reference to the inverter neutral point N:

$$u_{XNex}^*(t) = \left[\left| u_{Xref}^*(t) \right| + \frac{1}{2} \left(\text{sgn} \left(\left\{ \left| u_{Xref}^*(t) \right| \right\} - u_{carr}^*(t) \right) + 1 \right) \right] \times \text{sgn} \left(u_{Xref}^*(t) \right), \quad (3)$$

where u_{Xref}^* is the relative value of the reference instantaneous phase voltage u_{Xref} ; u_{carr}^* is the only carrier signal with the peak-to-peak amplitude equal to the unite; $|w|$ is the absolute value of w ; $\lfloor w \rfloor$ means the rounding down w to the closest integer number, taking into account the sign (the "floor" function); $\{w\}$ means the fractional part of w , i.e. $\{w\} = w - \lfloor w \rfloor$;

$$\text{sgn}(w) = \begin{cases} -1 & \text{if } w < 0 \\ 0 & \text{if } w = 0 \\ 1 & \text{if } w > 0. \end{cases}$$

To simulate the same well-known voltage signals of POD as we can obtain by applying the circuit of Fig. 3, we need only to modify this circuit for the use of (3). The modification itself is consisting in merely replacing the triangle carriers signals with the signals for dividing levels, as is shown in Fig. 5. Here each of the "X" phase output voltage executed signals, u_{XNex}^* or u_{XNex} , can be employed as the modulating phase voltage signal.

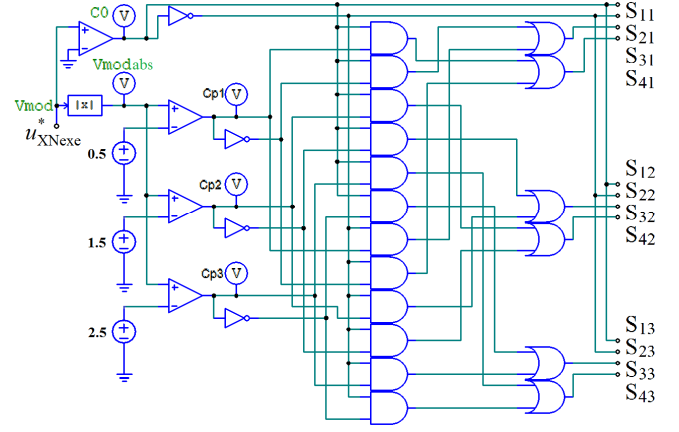


Fig. 5. Modified PSIM-model of phase "X" switches' control interface of three-phase seven-level cascaded H-bridge inverter.

Some kinds of space vector PWM are exactly oriented to the executed voltage signals obtaining [16, 17].

The baseline principle of the voltage waveform shaping of the recently offered quarter-wave-symmetric space vector PWM (QWS-SVPWM) is the two-component generating of the executed voltages' signals, initially for the delta voltages [16]:

$$u_{XYex}^*(t_{ks}) = \lfloor u_{XYrefks}^* \rfloor + f_{XYex}(t_{ks}), \quad (4)$$

where $u_{XYex}^*(t_{ks})$ is being executed during the clock cycle (with current time t_{ks}) for the sampling with number k , $k = 1 \dots m_f$, so each output (modulating) period with duration T corresponds to m_f clock-cycle periods with duration T_c , here m_f is the frequency modulation index,

$$m_f = f_c / f = T / T_c, \quad (5)$$

f_c and f are the clock-cycle and modulating frequencies, respectively; $u_{XYrefks}^*$ is the reference value sampled for the midpoint of the clock cycle interval with number k .

The decomposition (4) provides low-frequency commutations of the power switches. To see the full description of the QWS-SVPWM technique, please refer to [16]. The QWS-SVPWM simulated voltages' waveforms and dependences of selected harmonic coefficients on the amplitude modulation index are shown in Fig. 6 and Fig. 7, respectively. They have been obtained directly through the use of the PSIM model of Fig. 1 and Fig. 5 with the supplementary QWS-SVPWM functional unit.

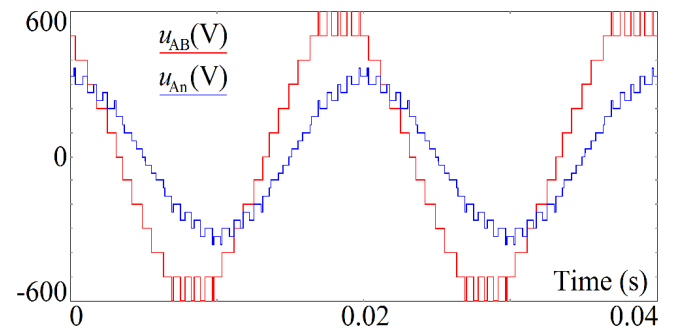


Fig. 6. Example of MLVSI output delta and phase voltages' PSIM-simulated waveforms for QWS-SVPWM algorithm.

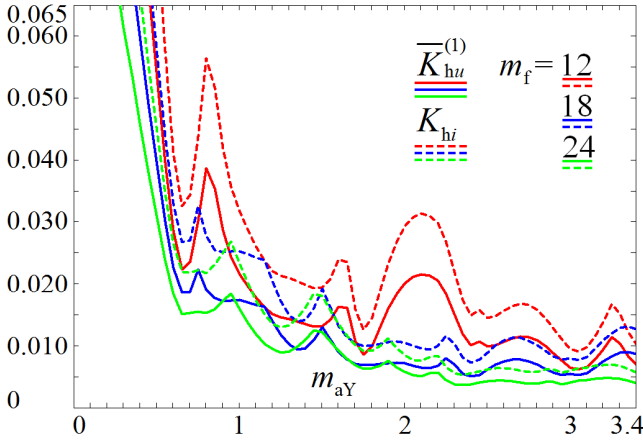


Fig. 7. First-order IHF of MLVSI phase voltage $\overline{K}_{hu}^{(1)}$ and load current's harmonics factor K_{hi} of PSIM-simulated waveforms for QWS-SVPWM algorithm versus phase voltage amplitude modulation index.

The waveforms of Fig. 6 correspond to the particular control parameters, $m_f = 24$ and $m_{aY} = 3.2$, here m_{aY} is the phase voltage amplitude modulation index,

$$m_{aY} = U/U_d = U^*, \quad (6)$$

U and U^* are the value and relative value of the reference voltage space vector magnitude (reference phase voltage amplitude value).

Fig. 7 is related to the PSIM power circuit model of Fig. 1 under the following parameters of all the three phases: $R = 48.13 \text{ Ohm}$ and $L = 0.14 \text{ H}$ (a simplified imitation of an three-phase induction motor steady-state mode). As can be seen, the PSIM model makes it possible to assess the inverter output current quality. The obtained dependence of the load current's harmonics factor K_{hi} (THD) is changing similarly to the one of the phase voltage's first-order integrated voltage harmonics factor (IHF) $\overline{K}_{hu}^{(1)}$ (also called the first-order weighted THD) [18]. This essentially validates the possibilities of the model in the optimization of the MLVSI load current's THD through the investigation of both the current itself waveform and the MLVSI voltage waveform.

IV. COMMON-MODE VOLTAGE MINIMIZATION

A common-mode voltage (CMV) problem is a serious scourge of AC electric drive systems based on PWM-modulated voltage source inverters (see, for example, [19]).

The CMV of any three-phase MLVSI circuit can be treated as the voltage across the common points of the load and of the supplying system (n and N respectively), and it is being calculated as follows:

$$u_{nNex}^*(t) = \frac{u_{ANex}^*(t) + u_{BNex}^*(t) + u_{CNex}^*(t)}{3}, \quad (7)$$

where u_{XNex} is the phase "X" executed voltage, referred to the node N.

The possible way to eliminate the three-phase CMV is to apply the particular MLVSI voltage space vectors, which produce the zero CMV value (see, for example, [20]).

However, avoiding the vectors with non-zero u_{nNex}^* value significantly degrades the harmonic content of the shaped voltage and decreased the linear range of the voltage amplitude modulation index [17]. Thus, the full set of vectors applying, while limiting the CMV value, is the most winning strategy and the direction of many studies.

Thorough analysis of the voltage space vectors of the vector diagram in Fig. 2 through the prism of (7) has made it possible to determine the accessible minimums of $u_{nNex}^*(t)$ values at every moment of time (i.e. as an instantaneous function):

$$\begin{aligned} u_{nNexmin}^*(t) &= A(t) + B(t), \\ A(t) &= -\left\{ \frac{u_{BCex}^*(t) - u_{ABex}^*(t)}{3} \right\}, \quad B(t) = \lfloor \lfloor C(t) \rfloor / C(t) \rfloor, \\ C(t) &= \frac{u_{BCex}^*(t) - u_{ABex}^*(t) + b + 1}{3}. \end{aligned} \quad (8)$$

Here b is a biasing number, which must meet the conditions:

- 1) $b = 3n$, n is a natural number;
- 2) $b \geq 2 \cdot (N - 1)$, N is the number of MLVSI levels.

Now we should specify the values of the phase executed voltages with reference to the inverter neutral point N for providing the condition of the minimum CMV value:

$$\begin{aligned} u_{BNex}^*(t) &= u_{nNexmin}^*(t) - \frac{u_{ABex}^*(t) - u_{BCex}^*(t)}{3} = \\ &= \frac{3u_{nNex}^*(t) - u_{ABex}^*(t) + u_{BCex}^*(t)}{3}, \\ u_{ANex}^*(t) &= u_{BNex}^*(t) + u_{ABex}^*(t), \\ u_{CNex}^*(t) &= u_{BNex}^*(t) - u_{BCex}^*(t). \end{aligned} \quad (9)$$

The resulting voltages' waveforms for the PSIM model of the baseline QWS-SVPWM technique [21], supplemented by the circuit of Fig. 5 and by the circuit unit, implementing (8) and (9), are shown in Fig. 8 for the control parameters $m_f = 24$ and $m_{aY} = 2.6$. The power circuit voltages' signals correspond to $U_d = E = 100 \text{ V}$.

A series of computer model experiments with the considered full PSIM model confirm that the CMV value is limited within the expected range,

$$u_{nNex}^*(t) = u_{nNexmin}^*(t) \leq 1/3, \quad u_{nN} \leq U_d/3, \quad (10)$$

while changing the amplitude modulation index over the entire range. In other words, each voltage space vector from the full set of vectors of the MLVSI space vector diagram corresponds to its minimum in absolute value CMV normalized value from the set $\{-1/3, 0, 1/3\}$. Such the CMV values limitation mitigates the CMV problem and simplifies measures to protect against the undesirable phenomena.

The results obtained confirm that PSIM simulation, if not a serious competitor to simulation in MATLAB-Simulink, is an excellent tool with the widest possibilities for the initial stage of power electronics circuits modeling and design.

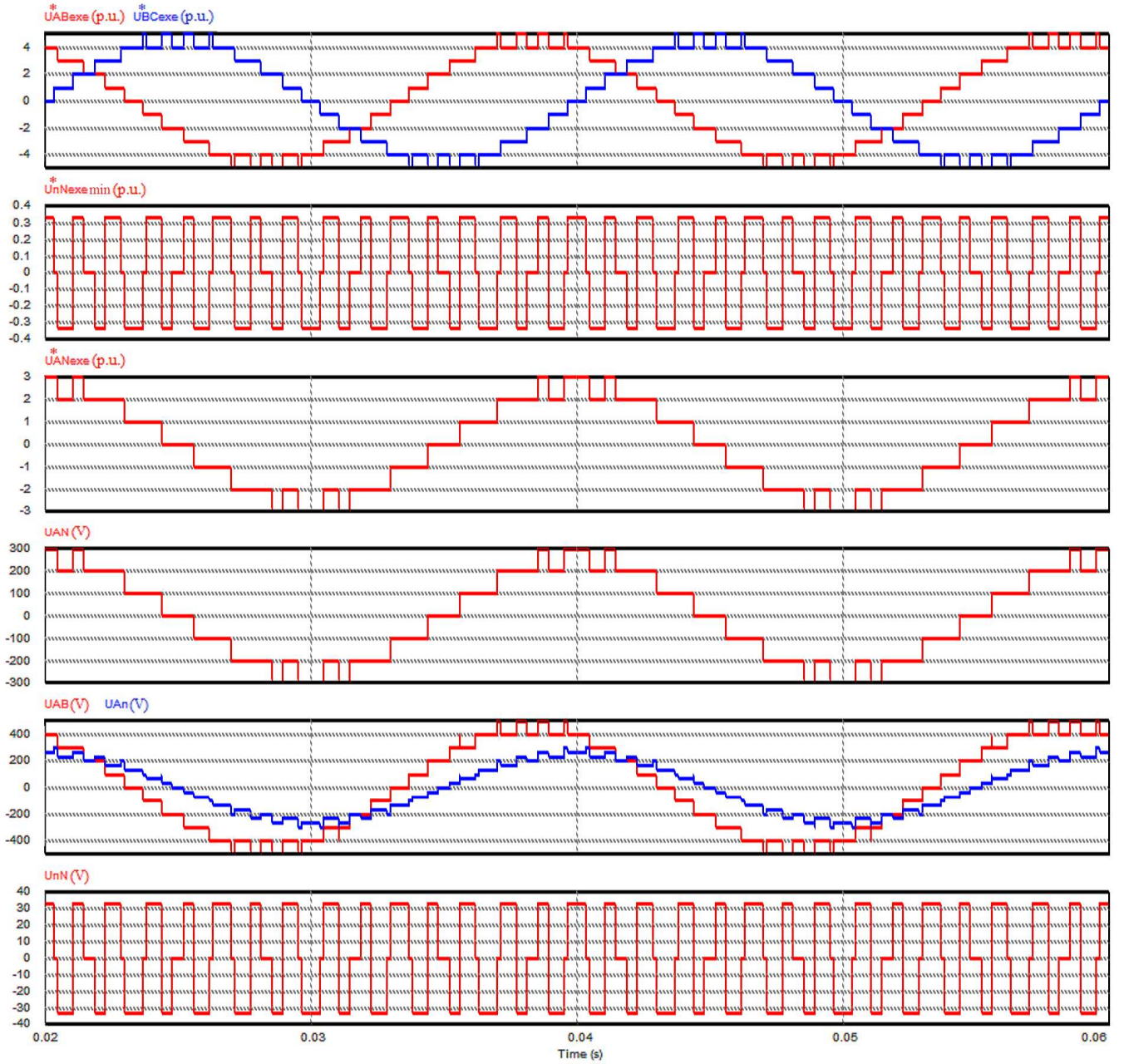


Fig. 8. Simulated waveforms of executed voltages' signals and power circuit voltages' signals of QWS-SVPWM-controlled MLVSI under the proposed supplementation to the technique.

V. CONCLUSION

The PSIM model of the seven-level cascaded H-bridge voltage source inverter, including a control circuits of its power switches and intended for the investigation of the inverter output voltages and currents harmonic content quality is presented. A way of using this kind of PSIM models with minimum changes for simulation of multilevel voltage source inverters under both the carrier-based PWM and some kinds of space vector PWM is demonstrated. By way of illustration, some of the harmonic coefficients' dependences on the amplitude modulation index and of the signals' waveforms are shown.

The paper also proposes a way to reduce the common-mode voltage instantaneous value of a three-phase multilevel voltage source inverter (of any arbitrary topology and any arbitrary number of generated equal voltage levels) to the

level of one third of a base (unit level) value of the supplying direct voltage. The technique fits perfectly into the context of the recently proposed quarter-wave symmetric space vector PWM.

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