

New Implementation of Common-Mode-Voltage-Eliminating Nearest-Vector-Selecting Space Vector Control for Three-Phase Multilevel Inverter

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Abstract—A simpler implementation of the space vector control technique, which is selecting the vectors nearest to the reference, and whereby providing elimination of the common-mode voltage of three-phase multilevel voltage source inverters (MLVSI) is proposed. The considered algorithm applies the particular MLVSI voltage space vectors, which produce the zero value of the common-mode voltage, i.e. the voltage across the load common point and the MLVSI common point. Two normalized inverter phase voltages values (star load voltages) have been projected to the new oblique-angled 60-degree axes. These values are treated not only as the oblique-angled coordinates, but also as barycentric coordinates on triangles of three nearest zero-common-mode-voltage vectors. The offered approach helps to get rid of the drawback of the conventional implementation of the space vector control with elimination of the common-mode voltage. In particular, no multiple applying per sampling period the square function and the square root function, related to distances calculations, are needed.

Keywords—three-phase multilevel voltage source inverter, voltage space vector control, nearest vector selecting, common-mode voltage elimination, barycentric coordinates, oblique-angled coordinates, integer and fractional parts of voltages normalized values

I. INTRODUCTION

Multilevel voltage source inverters (MLVSI) [1, 2] are now the most promising three-phase AC power generating systems from the point of view of both the level of output power and the quality of it. Numerous publications confirm MLVSI readiness to a wide range of industrial applications [3–7]. The variety of MLVSI circuitry solutions makes it possible to match a suitable option for applications with both high voltage and/or power values (such as a powerful electric drive, high power uninterruptible power supplies) and with high requirements for the limitation of higher harmonics content of voltage and load current waveforms (such as an accurate electric drive, uninterruptible power supplies with a nearly sinusoidal output waveform). One more intrinsic advantage of MLVSI compared to two-level inverters is the lowered voltage rating of the power semiconductor switches.

The two probably most used MLVSI circuits are shown in Fig. 1a and b.

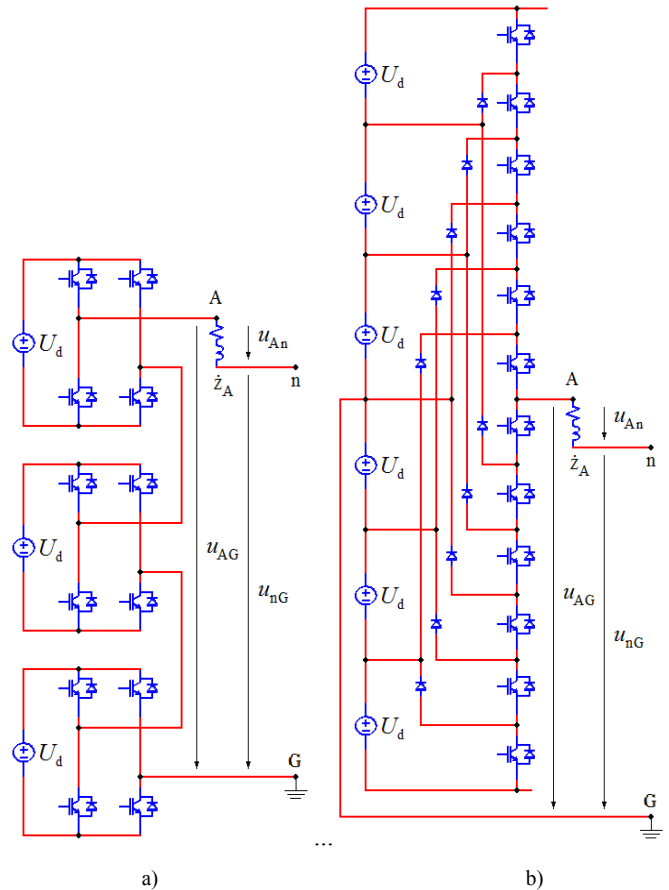


Fig. 1. One leg of simplified three-phase seven-level inverter circuit: a) cascaded transistor H-bridge inverter; b) diode clamped transistor inverter.

Here z_A is the phase A load impedance. The cascaded H-bridge (CHB) circuit needs no additional diodes compared the neutral-point-diode-clamped (NPC) circuit. But the 3-phase N -level CHB inverter requires 1.5 times more number of direct voltage sources than 3-phase N -level NPC inverter, $\frac{3}{2}(N-1)$ versus $N-1$. These two MLVSI circuits can be treated as the members of respective classes. The first class consists of MLVSI circuits that have an individual power supply for each

of the three phases and form a star of AC sources. Such circuits can be formed of single-phase circuits, e.g. cascaded or stacked structures. The second class consists of MLVSI circuits that supply the three phases from the same power source DC voltage levels. Their mid-points of DC buses are as a rule grounded. In addition to NPC circuits, flying capacitors inverters are the members of this class. Both MLVSI classes can generate the same output voltages' waveforms under the equal number of levels N .

II. IMPORTANCE OF THIS RESEARCH

The research is devoted to issues of MLVSI output power quality. Namely, one of control alternatives to PWM is considered to obtain common-mode voltage (CMV) elimination with enough low level both of higher harmonics content (of voltage and load current waveforms) and of semiconductor devices switching losses. The common-mode voltage problem is especially urgent for inverter-based systems [8, 9].

For any circuit of the three-phase MLVSI CMV is calculated as follows:

$$u_{nGex}^*(t) = \frac{u_{AGex}^*(t) + u_{BGex}^*(t) + u_{CGex}^*(t)}{3}, \quad (1)$$

where u_{xG} is a phase voltage, referred to the node G; asterisks here and after indicate the normalized values, related to the unit direct voltage value U_d (base voltage level); each "exe" indicates the resulting control signal after applying the considered control technique. Its waveform must be replicated in an appropriate voltage of a power circuit.

Various typical solutions to reduce and eliminate CMV can be found in [3, 10, 11]. The MLVSI modulation technique is the most suitable instrument to provide high quality output AC power [2], [12], [13], including CMV elimination solution. Such control solutions are mostly belonging to various PWM modifications [14–18].

The space-vector approach provides the multitude of states and vectors under enough high number of MLVSI levels. The CMV problem complete overcoming is achievable when the zero-common-mode-voltage MLVSI voltage space vectors (ZCMVSV) are being used. They correspond to $u_{nGex}^* = 0$. The ZCMVSVs of a seven-level inverter in context of 60-degree oblique-angled coordinates of the phase-to-phase (delta) voltages' relative values are shown in Fig. 2. Space vector PWM (SVPWM) techniques applying ZCMVSVs are known at least since the early 2000's and now have reached an advanced and carefully developed level [19]. One of such techniques, the technique based on the recently offered quarter-wave-symmetric space vector pulse width modulation (QWS-SVPWM) algorithm [20], has been described and investigated in [21]. It is simple, keeps the quarter-wave symmetry of voltages' waveforms and can be adapted to any arbitrary topology.

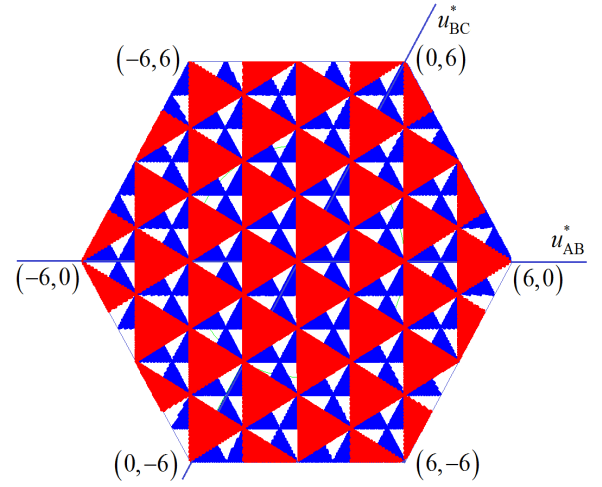


Fig. 2. Space-vector diagram with elementary triangles of zero-common-mode-voltage voltage space vectors of MLVSI in coordinates of normalized delta voltages values.

Despite the obvious general progress in PWM, any PWM in high power applications has disadvantage of high semiconductor commutation losses compared to ones under low-switching frequency modulation schemes like selective harmonic elimination, space vector control (SVC), nearest level control, modified nearest level modulation scheme [22]. Therefore, the searching of a control strategy, optimized from the point of view both low level of higher harmonics content of voltage and load current and low level of switching losses in semiconductor power switches is continued even for the techniques employing the whole set of the voltage space vectors¹. The SVC technique [23, 24] is probably the best low frequency alternative to PWM, but many researchers notice an increase of computational complexity with an increase in the number of levels of MLVSI. A modulation method to eliminate CMV in MLVSI, employing the ZCMVSVs [25] and based on [23, 24], is not without this disadvantage. Thus, it would be necessary to find a way to streamline implementation of common-mode-voltage-eliminating space vector control (with selecting the vector nearest to the reference one) for three-phase MLVSI.

III. PURPOSE OF PAPER

The above mentioned conventional SVC algorithm, applying ZCMVSVs [25], uses only the very closest ZCMVSV to the reference vector (RVSV) for the sample period. Its RVSV presentation is accomplished in orthogonal-components form, what can be written in terms of Fig. 1 and (1):

$$u_{ref}^o = u_{xref}^o + j \cdot u_{yref}^o,$$

$$u_{xref}^o = \frac{u_{xref}}{U_d} = u_{xref}^* = \frac{1}{3} (2 \cdot u_{AGref}^* - u_{BGref}^* - u_{CGref}^*),$$

1. N.N. Lopatkin, "Combined use of the nearest vector selecting technique and low-frequency quarter-wave symmetric space vector PWM in control of three-phase multilevel voltage source inverter," II Int. Theor. and Pract. Conf. on Alternative and Smart Energy (TPCASE 2020), IOP Conf. Series: Materials Science and Engineering, 2021, vol. 1035, 012020, pp. 1-10.

$$u_{yref}^{\circ} = \frac{u_{yref}}{U_d/\sqrt{3}} = \sqrt{3} \cdot u_{yref}^* = u_{BGref}^* - u_{CGref}^* \quad (2)$$

According to (2) the distances between RVSV sampled position and the two closest ZCMVSVs u_h° and u_l° (they should be determined by means of rounding functions) are calculated as follows:

$$d_h = \sqrt{3 \left(\text{Re}(u_{ref}^{\circ}) - \text{Re}(u_h^{\circ}) \right)^2 + \left(\text{Im}(u_{ref}^{\circ}) - \text{Im}(u_h^{\circ}) \right)^2},$$

$$d_l = \sqrt{3 \left(\text{Re}(u_{ref}^{\circ}) - \text{Re}(u_l^{\circ}) \right)^2 + \left(\text{Im}(u_{ref}^{\circ}) - \text{Im}(u_l^{\circ}) \right)^2} \quad (3)$$

Then the least value of d_h and d_l identifies a being executed ZCMVSV u_{exe}° , and its orthogonal coordinates u_{xexe}° and u_{yexe}° are being processed (again including rounding function applying) to obtain its phase voltages' coordinates u_{AGexe}^* , u_{BGexe}^* and u_{CGexe}^* [25].

The obvious drawback of the considered SVC algorithm is multiple applying per sampling period the square function and the square root function in (3) and rounding function. Fortunately, no distances calculations are needed if the barycentric coordinates' approach is employed for the nearest vector selecting space vector control implementation [26].

The purpose of the paper is to offer a new SVC technique with the common-mode voltage elimination for three-phase MLVSI, which is setting as the reference and processing as barycentric coordinates the phase load voltages projected to the new 60-degree oblique-angled axes. The developed Matlab/Simulink controller model and corresponding simulated idealized waveforms of the output voltages' signals are also presented in one of the subsequent sections.

IV. THEORY

The natural axes positions of the MLVSI phase voltages and phase-to-phase (delta) voltages are shown in Fig. 3. With the assumption of balanced load, it is advisable to consider the ZCMVSVs in coordinate frame of normalized values of MLVSI phase-to-neutral-point load voltages, as it is shown in Fig. 4.

Here the initial space vector diagram of Fig. 2 is rotated counterclockwise by 90 degrees. Also, the scale of the diagram is increased $2/\sqrt{3}$ times so that the side of the new elementary triangle corresponds to 1 of the relative phase voltage.

As can be seen from a comparison of Fig. 2 and Fig. 3, the u_{AB}^* and u_{BC}^* values in Fig. 2 are projected to the oblique-angled 60-degree axes. Probably, the first remarkable results in application of this kind of coordinates have been obtained in [27]. In a similar way to the above described, u_{Cn}^* and u_{An}^* values are projected in Fig. 4 to the new oblique-angled 60-degree axes, and RVSV processing has been implemented in coordinates (u_{Cn}^*, u_{An}^*) .

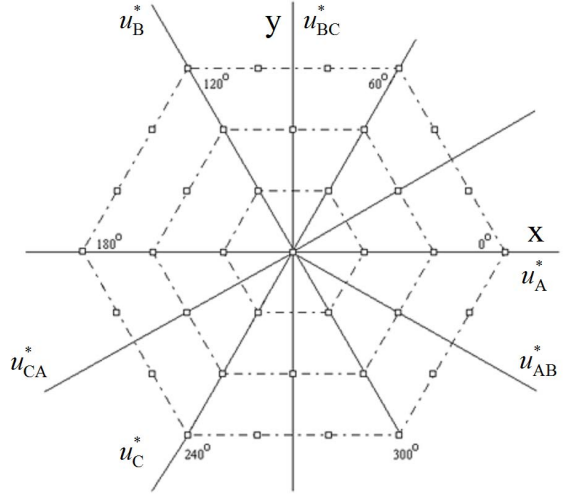


Fig. 3. Natural axes positions of phase voltages and delta voltages of three-phase MLVSI.

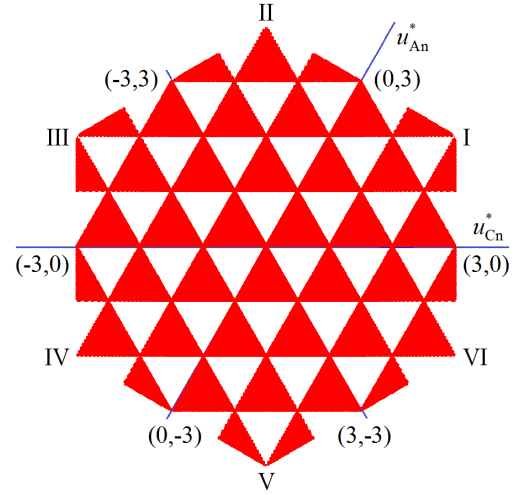


Fig. 4. Space-vector diagram with elementary triangles of zero-common-mode-voltage voltage space vectors of MLVSI in new coordinates of normalized phase voltages values.

Similar to the baseline QWS-SVPWM algorithm [20] and the common-mode-voltage-eliminating space vector pulse width modulation (CMVE-SVPWM) algorithm [21], proposed common-mode-voltage-eliminating space vector control (CMVE-SVC) technique uses the two-component principle of the executed voltages shaping. For some sampling moment each of the two output phase-to-ground voltages is calculated as follows:

$$u_{XGexe}^* = u_{Xnexe}^* = \lfloor u_{Xnref}^* \rfloor + f_{Xnexe}, \quad (4)$$

where u_{Xnref}^* is the sampled reference voltage signal; $\lfloor x \rfloor$ is the floor function of x ; f_{Xnexe} can possess the only values 0 and 1.

Such approach specifies for execution the rhombus of two potential triangles of the nearest to the reference RVSV vectors

(NTV), see Fig. 5, where $\{u_{Xn}^*\}$ means the fractional part of u_{Xn}^* , $\{u_{Xn}^*\} = u_{Xn}^* - \lfloor u_{Xn}^* \rfloor$ (here and after “ref” and “exe” are omitted in the subscripts of some interim values). These fractional parts are not only the duty cycles values of the NTVs over the SVPWM clock cycle [20, 21]. They are the barycentric coordinates as well which are specified by reference to the NTV triangle. The maximum barycentric coordinate of the three ones indicates the space vector to be chosen [26].

Taking into account $\{-u_{Xn}^*\} = 1 - \{u_{Xn}^*\}$ for non-integer u_{Xn}^* values, one can derive simple logical expressions

$$\begin{aligned} f_{Cnexe} &= (F_{up} \cap f_{Cn1} \cap f_{Cn2}) \cup (\bar{F}_{up} \cap (f_{Cn1} \cup f_{Cn2})) \\ f_{Anexe} &= (F_{up} \cap f_{An} \cap \bar{f}_{Cn1}) \cup (\bar{F}_{up} \cap (f_{An} \cup \bar{f}_{Cn1})) \end{aligned} \quad (5)$$

where F_{up} is the upward-pointing triangle kind identifier [20]; $\bar{w}$ is the inverse of w ;

$$\begin{aligned} f_{Cn1} &\equiv \{u_{Cn}^*\} > \{u_{An}^*\} \\ f_{Cn2} &\equiv \{u_{Cn}^*\} > \{u_{Bn}^*\} \\ f_{An} &\equiv \{u_{An}^*\} > \{u_{Bn}^*\} \end{aligned}$$

After determining the values of u_{CGexe}^* and u_{AGexe}^* according to (4), the third phase-to-ground voltage can be calculated, taking into account $u_{nGexe}^* = 0$ and (1):

$$u_{BGexe}^* = -(u_{CGexe}^* + u_{AGexe}^*). \quad (6)$$

Based on (4)–(6) Matlab/Simulink controller model will be dealt with further on.

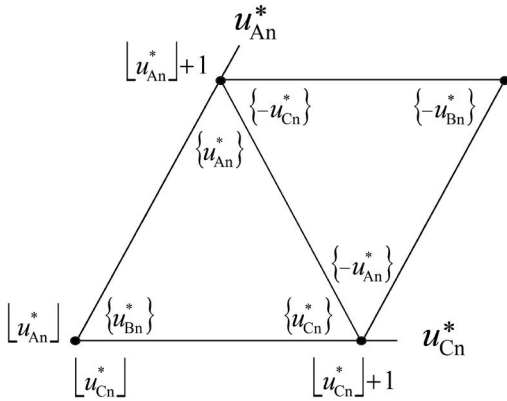


Fig. 5. Coordinates and barycentric coordinates (on NTV triangles) of zero-common-mode-voltage space vectors.

V. SIMULATION RESULTS

The considered here controller model of instantaneous common-mode-voltage-eliminating SVC nearest-vector-selecting space vector control is obtained from the respective one for SVC new implementing technique on full set of vectors [26] almost only by replacing the delta voltages with the relevant star voltages, namely, u_{AB}^* with u_{Cn}^* , u_{BC}^* with u_{An}^* and u_{CA}^* with u_{Bn}^* .

The resulting model (prepared in Simulink) is shown in Fig. 6. Here $b_{Xn} = \{u_{Xn}^*\}$, m_{aY} is the index of the amplitude modulation of a phase voltage,

$$m_{aY} = U/U_d = U^*, \quad (7)$$

U and U^* are the value and normalized magnitude value of the RVSV.

The blocks denoted by u_{XGexe}^* generate the respective executed signals for phase legs to be replicated as power circuit voltages. Here the analog variant of the SVC is implemented. It corresponds to the sampling interval which approaches zero. The impact of the reference voltages sample rate on the SVC output voltages higher harmonics content can be easily assessed².

The idealized simulated CMVE-SVC oscillograms of the phase-to-neutral voltage u_{An}^* (which is equal to corresponding phase-to-ground voltage u_{AG}^*) and phase-to-phase (delta) voltage u_{BC}^* are shown in Fig. 7 and Fig. 8 for values of the index of the amplitude modulation 3.5 and 12.6, respectively.

Thus, the waveforms of space vector control technique with the elimination of the common-mode voltage are really implemented in the model. Presenting the THD and weighted THDs estimates is the subject of separate paper. As can be seen from Fig. 7 and Fig. 8 comparing, the rising number of MLVSI levels eliminates the problem of the output voltages waveforms quality.

VI. CONCLUSION

The new implementation of the space vector control with the nearest vector selection for elimination of the common-mode voltage is proposed for three-phase multilevel voltage source inverters. The considered technique applies the particular MLVSI voltage space vectors, which produce the zero value of the common-mode voltage, i.e. the voltage across the load common point and the MLVSI common point. The presented technique uses both the integer parts and the fractional parts of the reference phase voltages' normalized values as the coordinates and barycentric coordinates (specified by reference to the NTV triangle) of the reference space vector. Since no distances calculations are needed, the multiple-applied per sampling period the square function and the square root function have been completely removed. The presented controller model confirms the simplicity of all the necessary calculations.

2. N.N. Lopatkin, "Assessment of output voltage quality of three-phase multilevel inverter with nearest vector selecting space vector control," 14th Int. Sci.-Tech. Conf. on Actual Problems of Electronics Instrument Engineering (APEIE), 2018, Vol. 1, part 6, pp. 158-163.

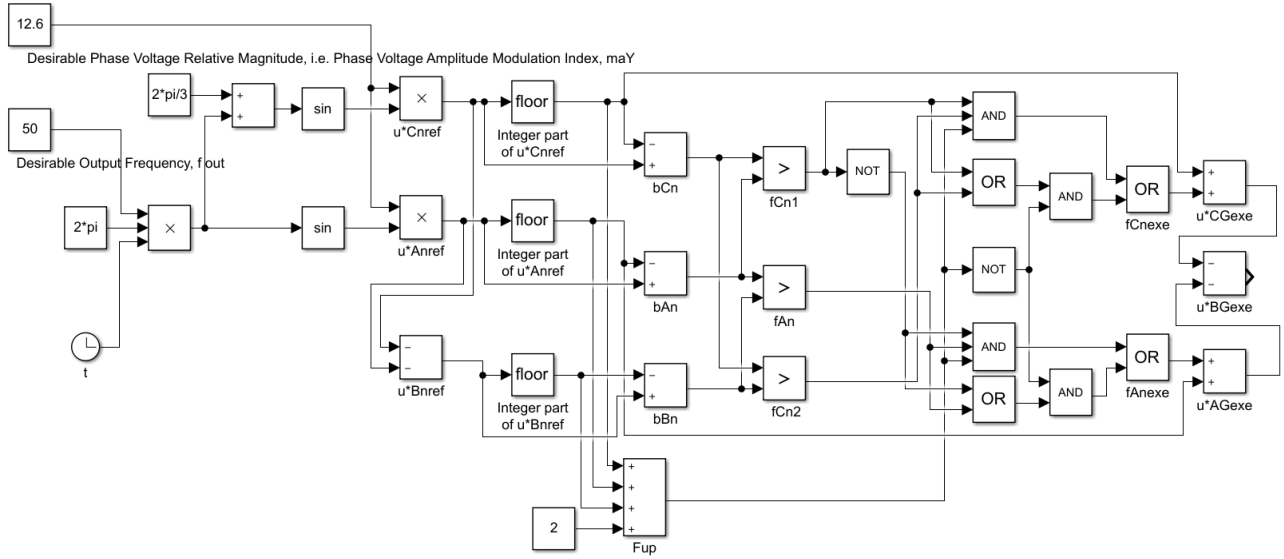
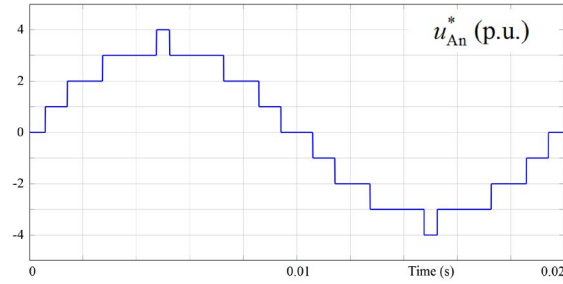
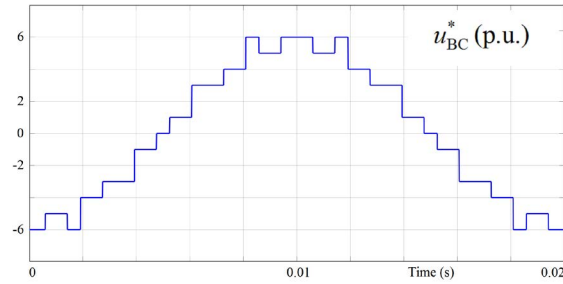


Fig. 6. New common-mode-voltage-eliminating nearest voltage vector selecting controller for arbitrary circuit and level number three-phase MLVSI in linear mode.

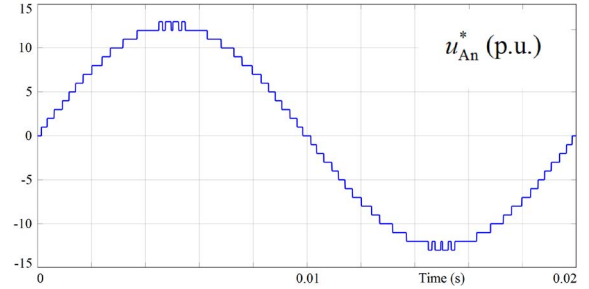


a)

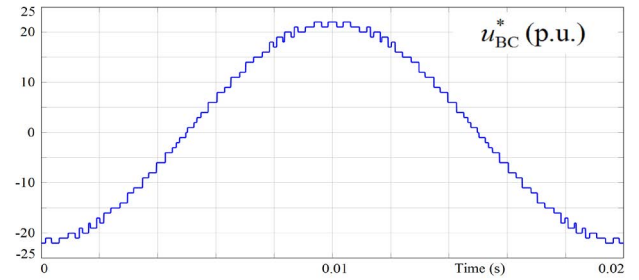


b)

Fig. 7. Simulink-simulated waveforms of MLVSI voltages for $m_{aY} = 3.5$: phase voltage a), delta voltage b).



a)



b)

Fig. 8. Simulink-simulated waveforms of MLVSI voltages for $m_{aY} = 12.6$: phase voltage a), delta voltage b).

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