

Integrated Voltage Harmonics Factors Estimation of Multilevel Voltage Source Inverter with Common-Mode-Voltage-Eliminating Space Vector PWM

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Abstract—The harmonics-related performance characteristics of the common-mode-voltage-eliminating space vector pulse width modulation (CMVE-SVPWM) technique for three-phase multilevel voltage source inverter (MLVSI), based on the recently offered quarter-wave-symmetric space vector pulse width modulation (QWS-SVPWM) algorithm, are investigated. Namely, the dependences of the output voltage THD and three low-order weighted THDs values on the phase voltage amplitude modulation index are obtained by LabVIEW simulation for the three low, multiple of 12, values of frequency modulation index and the considerably extended range of the amplitude modulation index. Like the baseline QWS-SVPWM algorithm, the CMVE-SVPWM technique keeps the quarter-wave symmetry of the star (phase-to-neutral) and delta (phase-to-phase) voltages and is intended for MLVSI of any arbitrary topology with any arbitrary number of generated equal voltage levels. The zero-common-mode-voltage MLVSI space vectors are being applied, producing the zero value of the voltage across the neutral point of the load and the inverter system ground point. To this end, relative values of the MLVSI phase load voltages, referred to the three-phase load common star point (phase-to-neutral load voltages) are being set as the reference ones and being processed.

Keywords—three-phase electric power, DC-AC power converters, voltage source inverters, multilevel inverters, space vector pulse width modulation, power quality, common-mode voltage, total harmonic distortion, integrated voltage harmonics factors, weighted total harmonic distortion.

I. INTRODUCTION

A vast majority of industrial AC electric drives employ as power electronics converter unit for power and control the various kinds of voltage source inverters (VSI) with pulse-width modulation (PWM) of their output voltages. This allows for the high quality control of AC motors speed and torque, the optimization of technological processes and operating modes of electro-mechanical drive systems [1, 2].

Multilevel VSI (MLVSI) circuits have become a breakthrough technology in both the high-power medium-voltage and high-voltage AC drives and the precision AC drives [3-12] thanks to the possibility of increasing the magnitudes and improving the waveforms of the generated voltages at fixed voltage values across power semiconductor switches. Simultaneously, various multilevel PWM techniques for MLVSI have been being developed and improved for more than twenty years (for instance, see the above mentioned references and [13, 14]).

However, PWM is not only the flexible and convenient control tool, but also the cause of an exacerbation of a common-mode voltage (CMV) problem.

The CMV of a three-phase AC system can be generally defined as the voltage u_{nG} across a load neutral point n and a whole system ground point G . The CMV related to MLVSI circuits is shown in Fig. 1 for two different cases of the ground point position.

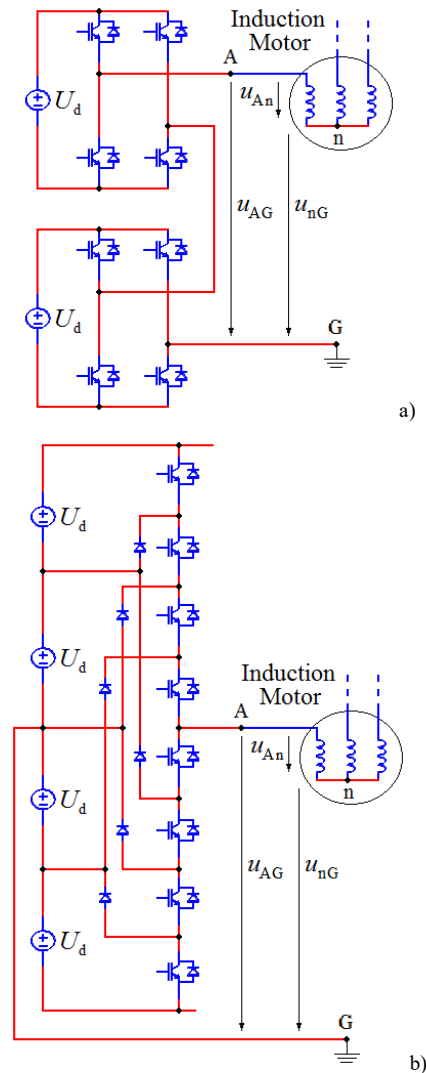


Fig. 1. Common-mode voltage in three-phase five-level inverters feeding star-connected induction motors: a) in cascaded H-bridge circuit; b) in neutral point clamped circuit.

Fig. 1,a corresponds to the MLVSI circuits' kind, having a separated per phase supplying and forming a three-phase star-connected AC source with a grounded neutral point (a common star point). The cascaded H-bridge (CHB) topology MLVSI is shown here as the typical and the most frequently used member of this category of MLVSI. The other MLVSI circuits, using the same power source DC voltage levels for all the three phases, have the central point of the sectioned DC voltage source (DC bus mid-point) as the system ground point G. The most known and used types of this MLVSI category are the so-called diode clamped or neutral point clamped (NPC) topology (see Fig. 1,b) and flying capacitors (FC) topology.

For the both three-phase MLVSI circuits' categories, taking into account the different location of their nodes G, the being executed three-phase CMV value can be expressed via phase voltages u_{XG} (which are referred to the node G) as follows:

$$u_{nGex}^*(t) = \frac{u_{AGex}^*(t) + u_{BGex}^*(t) + u_{CGex}^*(t)}{3}, \quad (1)$$

where asterisks in the superscripts designate the relative (normalized) values $u_{XY}^* = u_{XY}/U_d$, U_d is the direct voltage of the unit (base) level; here and after "exe" in the subscripts designates the executed signals and power circuit voltages, whose waveforms are the results of the considered technique applying.

A CMV in both single-phase and three-phase AC power systems is the source of many undesirable phenomena, which are particularly urgent in AC electric drive systems. These are leakage currents through parasitic elements, shaft voltage and bearing currents in AC motors, and they can bring in negative consequences and result in reducing the efficiency and reliability of the power supplying and service lives of the system components. In addition to equipment malfunctions, improper operations of automation due to a CMV, causing decline in the quality of the generated voltage and electromechanical performance characteristics, there may be a risk of electric shock to service personnel.

As has been pointed out, the CMV problems are especially actual in inverter-based systems [15, 16], including transformerless photovoltaic AC power supplies [17]. Regarding three-phase MLVSI circuits, the CMV reduction and elimination is the problem, common to all of the topologies, and attracting many researchers. Like to solutions for single-phase inverters, all the CMV-mitigating measures in three-phase inverter-based systems can be roughly divided into circuitry, control and mixed solutions [4]. Among the applied hardware means there are special-designed external passive and active common-mode filters and special inverter topologies [18,19]. But typical common-mode noise filters are bulky, expensive and reducing a system efficiency. The special topologies are mostly oriented to low-level inverters, since MLVSI circuits a priori have a reduced amplitude and voltage transition step of the CMV.

The control solutions are generally based on advanced PWM techniques [13, 14, 20-27], including modified sinusoidal PWM technologies. In case of MLVSI applying, space vector PWM (SVPWM) techniques provide a rich choice of switching states and generated voltage space vectors (SV), therefore the CMV can be completely

eliminated due to selecting and using particular SVs. Additionally, the rising number of MLVSI levels eliminates the problem of the output power quality declining and makes it possible to reduce AC motors' electromagnetic torque pulsations. In some instances, the project designers request extremely high, by today's industrial standards, levels' number. In particular, a designed trinary hybrid 81-level inverter for motor drive with zero common-mode voltage is presented in [6].

The using zero-common-mode-voltage space vectors (ZCMVSV) technique, based on the recently offered quarter-wave-symmetric space vector pulse width modulation (QWS-SVPWM) algorithm [28], has been proposed in [29]. Here and after any ZCMVSV should be treating as SV corresponding to $u_{nGex}^* = 0$ under CMV definition by (1).

The PSIM-simulated power circuit waveforms demonstrated the unavoidable degradation of the quality of the generated output power compared to the waveforms related to the entire set of the MLVSI space vectors in the initial range of the phase voltage amplitude modulation index values.

The purpose of this paper is to provide the dependences of the output voltage THD and three low-order integrated voltage harmonics factors (IHF) [30] values, i.e. the weighted THDs values, on the phase voltage amplitude modulation index for the considerably extended range of the latter. Here the value of the amplitude modulation index is not limited by the PSIM power circuit model, since the idealized executed voltage signal waveforms are obtained in LabVIEW modulator model. The corresponding higher harmonics content assessment is performed by means of the specially developed virtual instrument [31].

II. CONCISE DESCRIPTION OF NEW COMMON-MODE-VOLTAGE-ELIMINATING SPACE VECTOR PWM TECHNIQUE

There are many described techniques, using the zero-common-mode-voltage space vectors, both in classical researches of widely known specialists and recent publications. As examples, advanced developments in [32, 33] can be pointed. However, the considered here technique, intended for MLVSI of any arbitrary topology, seems to be having advantage, since it keeps its computation simplicity for any arbitrary number of generated equal voltage levels.

The new common-mode-voltage-eliminating space vector PWM (CMVE-SVPWM) technique is based on the QWS-SVPWM algorithm, which operates with the relative values (in the sense announced after (1)) of the phase-to-phase (delta) voltages as the coordinates in the context of the 60-degree oblique-angled axes [28], see Fig. 2,a. Similarly, CMVE-SVPWM technique operates in the context of the 60-degree oblique-angled axes with the relative values of the phase (star) voltages, related to the load, i.e. referred to the three-phase load common star point [29], see Fig. 2,b. The values u_{Cn}^* and u_{An}^* in Fig. 2,b have been projected to the new axes in a similar way as it had been done in Fig. 2,a for the values u_{AB}^* and u_{BC}^* .

The zero-value condition for the executed CMV voltage, $u_{nGex}^*(t) = 0$, means that each referred to the system ground point G phase voltage should be equal to the respective phase load voltage (referred to the common star point n).

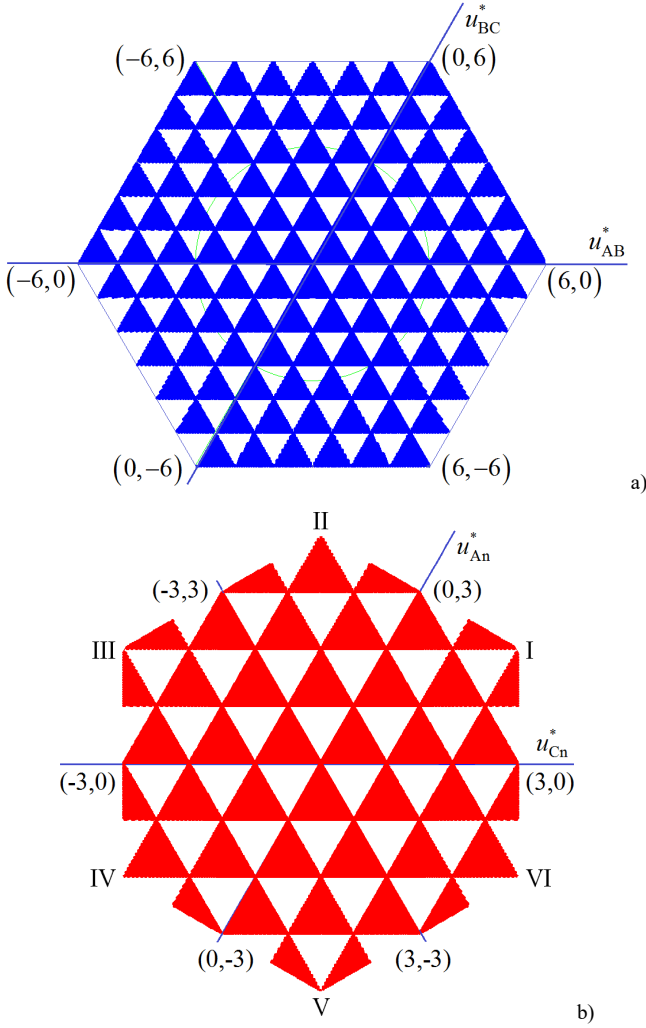


Fig. 2. Space vector diagrams with triangles of the three nearest voltage vectors of three-phase multilevel inverter (here levels' number is seven): a) entire set of space vectors in coordinate frame of relative values of delta voltages; b) set of zero-common-mode-voltage space vectors in coordinate frame of relative values of load phase voltages.

Thus, in view of the fact that the executed phase-to-neutral-point-n voltages $u_{Xnexe}^*(t)$, $X \in \{A, B, C\}$, are assumed to be symmetric, i.e. the three-phase load is supposed to be balanced, the following conditions should be valid:

$$u_{XGex}^*(t) = u_{Xnexe}^*(t), \quad u_{AGex}^*(t) + u_{BGex}^*(t) + u_{CGex}^*(t) = 0. \quad (2)$$

The proposed PWM technique is the regular sampled one, namely each output (modulating) period with duration T corresponds to m_f clock-cycle periods with duration T_c , here m_f is the frequency modulation index,

$$m_f = f_c / f = T / T_c, \quad (3)$$

where f_c and f are the clock-cycle and modulating frequencies, respectively.

The above mentioned phase-to-neutral load voltages are being set as the reference ones to be processed, namely the sampled values $u_{Xnrefsk}^*$ for the midpoint of the clock cycle interval with number k are as follows:

$$u_{Cnrefsk}^* = m_{aY} \sin((2\pi k - \pi) / m_f + 2\pi/3),$$

$$u_{Anrefsk}^* = m_{aY} \sin((2\pi k - \pi) / m_f), \quad (4)$$

where m_{aY} is the phase voltage amplitude modulation index,

$$m_{aY} = U / U_d = U^*, \quad (5)$$

U and U^* are the value and relative value of the reference voltage space vector (RVSV) magnitude.

In accordance with the main shaping principle of the two voltages as the coordinates of the executed voltage space vector (EVSU) in the base QWS-SVPWM algorithm, each of the directly executed on the clock cycle interval k output phase-to-ground voltages are being formed as the two-component one:

$$u_{XGexek}^*(t_{kc}) = u_{Xnexe}^*(t_{kc}) = \lfloor u_{Xnrefsk}^* \rfloor + f_{Xnexe}(t_{kc}), \quad (6)$$

where $\lfloor x \rfloor$ means the rounding down x to the closest integer number, taking into account the sign (the “floor” function), so $\lfloor x \rfloor$ is the integer part of x ;

$f_{Xnexe}(t_{kc})$ is the pulse function, possessing the only values 0 and 1;

t_{kc} is the current time from the start of the clock cycle with number k , $t_{kc} = t - (k-1) \cdot T_c$, t is the total current time.

The durations of $f_{Xnexe}(t_{kc})$ pulses of the value 1 and the instants of time of their rising and falling edges are defined for each clock cycle interval k via the fractional values $\{u_{Xnrefsk}^*\} = u_{Xnrefsk}^* - \lfloor u_{Xnrefsk}^* \rfloor$ of the both sampled relative reference voltages, the sector number and the type of triangle of the three vectors which are the nearest to the RVSV reading (sample). The latter is being identified yet again through its coordinates $u_{Cnrefsk}^*$ and $u_{Anrefsk}^*$.

The unique and general three-segment switching sequence scheme for the three nearest vectors is the origin of the quarter-wave-symmetric waveforms of the output MLVSI phase and delta voltages in the both QWS-SVPWM and considered CMVE-SVPWM techniques. This scheme specifies the nature of the changes of the EVSV coordinates (u_{Cn}^*, u_{An}^*) and thus the quantities and positions of the $f_{Xnexe}(t_{kc})$ pulses.

The supplementary information one can find in [29] or in [28], and in the latter case, just by replacing all the variables, related to the delta voltages u_{AB}^* and u_{BC}^* , with the variables, related to the phase load voltages u_{Cn}^* and u_{An}^* , respectively.

After determining the values of $u_{CGexek}^*(t_{kc})$ and $u_{AGexek}^*(t_{kc})$ according to (6), the value of the last voltage function on the clock cycle k can be calculated, taking into account (2):

$$u_{BGexek}^*(t_{kc}) = -(u_{CGexek}^*(t_{kc}) + u_{AGexek}^*(t_{kc})). \quad (7)$$

At last, the obtained executed voltage functions $u_{AGexek}^*(t)$, $u_{BGexek}^*(t)$ and $u_{CGexek}^*(t)$ are being utilized as the reference functions to be reproduced at the MLVSI power circuit output.

For the N -level three-phase MLVSI under the proposed new CMVE-SVPWM control algorithm the maximum phase voltage amplitude modulation index value, corresponding to the limit of the linear range, can be calculated as follows:

$$U_{\max}^* = m_{aY\max} = \frac{1}{2}(N-1). \quad (8)$$

III. LABVIEW SIMULATIONS' RESULTS

The LabVIEW-implemented modulator model generates the continuous function for the clock cycle number $k(t)$ at first,

$$k(t) = \left\lfloor \left(\frac{t}{T} - \left\lfloor \frac{t}{T} \right\rfloor \right) \cdot m_f \right\rfloor + 1, \quad (9)$$

but the fractional value function $\{t/T\} = t/T - \lfloor t/T \rfloor$ is replaced by sawtooth wave, whose value grows from 0 to 1 within each output voltage period. The obtaining of the corresponding to (4) continuous time-dependent functions $u_{Xnrefs}^*(t)$ of two relative phase load voltages' reference signals, sampled and held in each clock cycle period, is shown in Fig. 3.

The resulting idealized executed waveforms of the MLVSI output phase-to-neutral voltage and delta voltage in Fig. 4 correspond to $m_f = 24$ and $m_{aY} = 5.9$. Here one can see that the low-frequency CMVE-SVPWM provides a quite low number of power transistors' switchings per period.

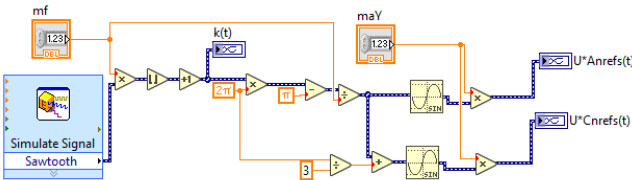


Fig. 3. Subcircuit for generation of two reference signals of relative values of load phase voltages as sampled and held in each clock cycle period.

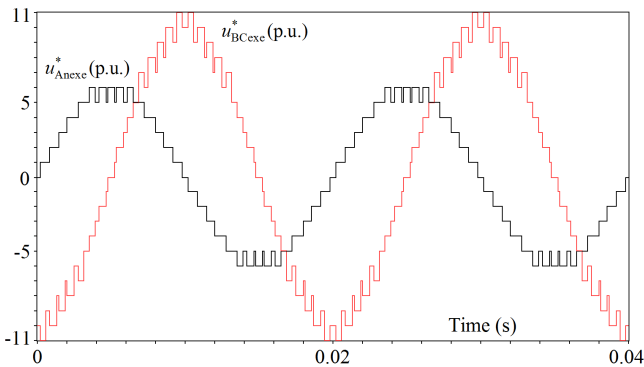


Fig. 4. Example of LabVIEW-simulated idealized modulator waveforms of output executed phase-to-neutral voltage and delta voltage.

The MLVSI load's current higher harmonics content, causing AC motor's electromagnetic torque pulsations, can be assessed by means of the value of the integrated voltage harmonics factor (IHF) $\bar{K}_{hu}^{(q)}$ with some order q related to respective q -order equivalent circuit of the motor and its filter [28, 30, 31]. Namely, the q -order IHF, also called q -order weighted THD (WTHD) factor, provides the estimate of relative harmonics content in a researched signal as though it is reduced after the action of the idealized q -order integrating electric circuit:

$$\bar{K}_{hu}^{(q)} = \frac{\bar{U}_{(hh)}^{(q)}}{\bar{U}_{(l)}^{(q)}} = \frac{\bar{U}_{(hh)}^{(q)} \cdot \omega^q}{U_{(l)}}, \quad (10)$$

where $U_{(l)}$, $\bar{U}_{(l)}^{(q)}$ and $\bar{U}_{(hh)}^{(q)}$ are the RMS value of the voltage fundamental component $u_{(l)}$ and RMS values of the results of the q times indefinite integral taking of the instantaneous values of the fundamental component $\bar{u}_{(l)}^{(q)}$, and of the high harmonics component $\bar{u}_{(hh)}^{(q)}$, respectively; ω is the fundamental angular output frequency, $\omega = 2\pi f$.

The voltage harmonics factor K_{hu} (voltage THD) can be treated as the zero-order voltage IHF, $K_{hu} = \bar{K}_{hu}^{(0)}$.

The LabVIEW modulator model and IHF-meter model make it possible to obtain zero- to three-order IHFs of the MLVSI output voltage for various values of m_f and m_{aY} . Here these IHFs' dependences on the phase voltage amplitude modulation index m_{aY} for the first values m_f , that are multiples of 12 (namely, 12, 24, and 36), are presented in Fig. 5 and Fig. 6 up to the $m_{aY\max} = 10$. So, the dependences reflect the voltage higher harmonics content for MLVSIs up to the 21-level circuit.

As can be seen, the frequency modulation index values 24 and 36 produce enough low voltage higher harmonics content, quite acceptable for many applications. And the number of the power transistors' switchings remains low as well, that can keep the efficiency value of some MLVSI circuit on a high level.

IV. CONCLUSIONS

The common-mode-voltage-eliminating space vector pulse width modulation technique for three-phase multilevel voltage source inverter of any arbitrary topology with any arbitrary number of generated equal voltage levels is considered. The zero-common-mode-voltage space vectors are being used, producing the zero value of the voltage across the neutral point of the load and the inverter system ground point. The above zero-common-mode-voltage vectors are being applied in accordance with all the attributes of the recently offered quarter-wave-symmetric space vector pulse width modulation, including the special three-segment switching sequence scheme for the three nearest vectors. The resulting waveforms of the inverter output phase and delta voltages are the quarter-wave-symmetric. In contrast to baseline algorithm, relative values of the inverter phase load voltages, referred to the three-phase load common star point (phase-to-neutral load voltages) are being set as the reference ones and being processed instead of the delta voltages.

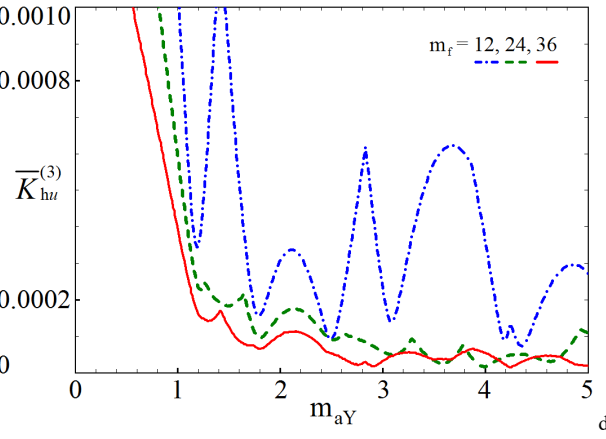
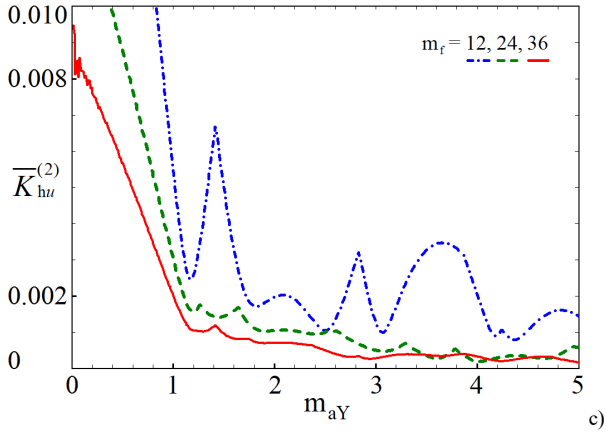
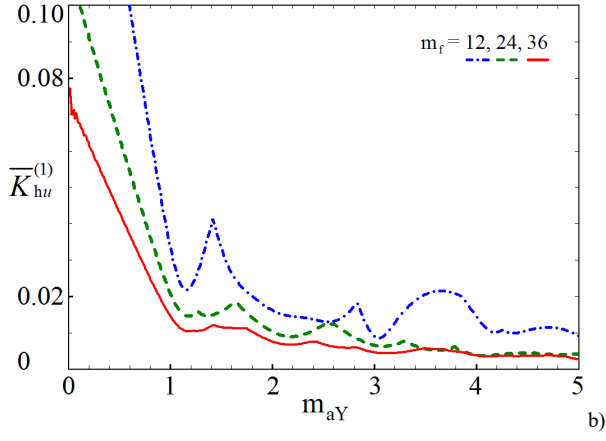
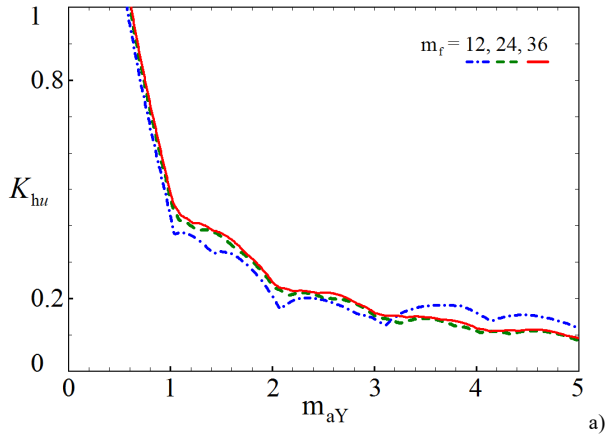


Fig. 5. LabVIEW-simulated THD (a) and first three orders IHF (b, c, and d) dependences on phase voltage amplitude modulation index m_{aY} in range $m_{aY} = 0 \dots 5$.

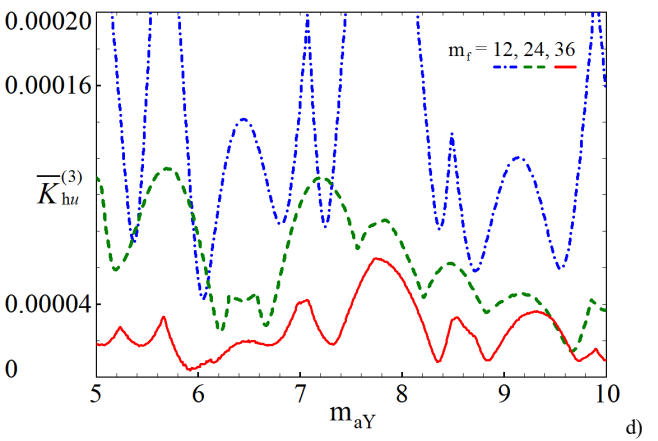
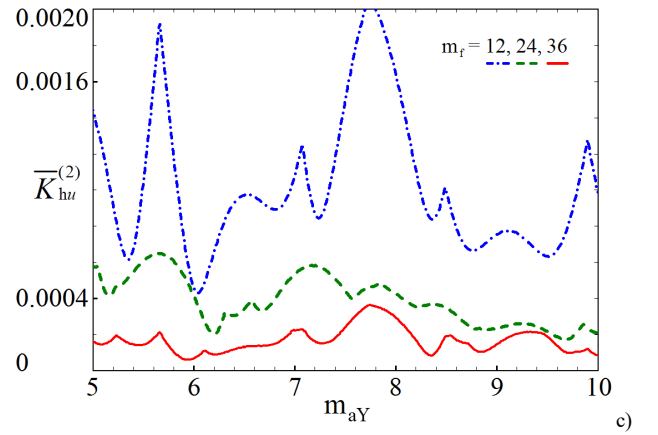
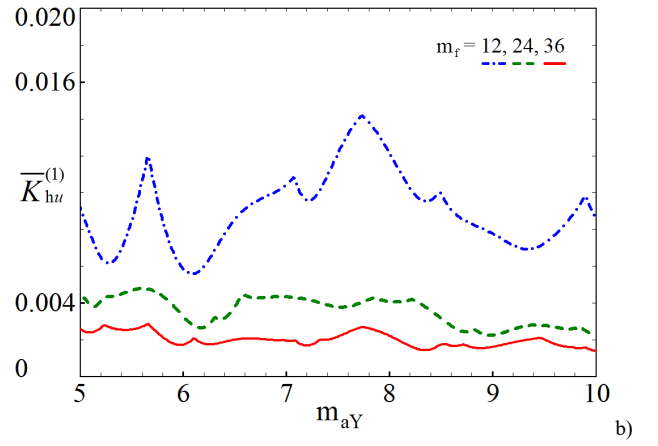
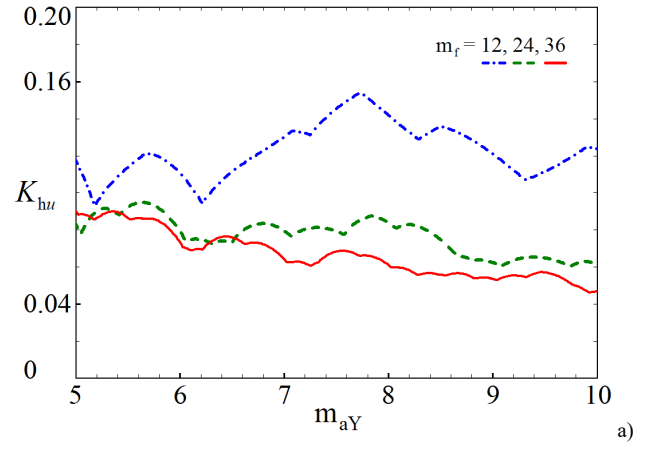


Fig. 6. LabVIEW-simulated THD (a) and first three orders IHF (b, c, and d) dependences on phase voltage amplitude modulation index m_{aY} in range $m_{aY} = 5 \dots 10$.

The dependences of the output voltage THD and three low-order weighted THDs values on the phase voltage amplitude modulation index are obtained by LabVIEW simulation for the three values of frequency modulation index and the considerably extended (up to value of 10) range of the amplitude modulation index. They confirm that the offered technique is promising from point of view of both the high quality of the generated voltages and the low level of dynamic losses in power semiconductor switches. The multilevel inverters' circuits controlled with the proposed method can be used in wide range of applications including both the high-power and precision AC drives.

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